REMARKS

Summary

Claims 30-43, 46-53, 78-80, 82, 101-131 are pending. Claims 72-77 and 81 have been withdrawn from consideration. Claim 30 is amended herein to recite at least one bonding layer comprising an amorphous material, and also crystallization of the amorphous material to a polycrystalline material during annealing. This amendment is supported in the specification at least in paragraphs [0065], [0066], and [0070]. Claims 33-35, 46, 49-51, 53, 82, 112, 114, 117, and 119 are amended to replace "bonding layer" or "layer" with "bonding layers" or "layers," consistent with the language in independent claim 30. Claim 39 is amended to correct a grammatical error. Claim 102 is amended herein to include the word "grown," which was inadvertently left out of the claim in the previous amendment. Claims 44 and 45 are cancelled herein to avoid redundancy, in view of the amendment to claim 30. Claims 120-131 are new, and are supported in the specification at least in paragraphs [0021], [0027], [0059], [0062], [0065], and [0071]. No new matter has been added.

Rejections Under 35 U.S.C. § 102

The Examiner asserted that claims 30-32, 36-42, 44-47, 49, 51-53, 78-80, and 101-104, 108-110, 112-114, 117-119 are anticipated by Lee et al. ("Lee," EP 1246238) under 35 U.S.C. §102(b). Applicants respectfully disagree in view of the amendment herein to independent claim 30 and the following remarks.

Claim 30

As amended, claim 30 recites that at least one of the bonding layers comprises an amorphous material and the annealing comprises crystallizing at least a portion of the amorphous material into a polycrystalline material. The Examiner incorrectly asserted in the previous Office action that the abstract of Lee disclosed annealing to form a polycrystalline material from an amorphous bonding layer. There is in fact no teaching in the abstract – or anywhere else in Lee – of *crystallizing* an *amorphous* material to a *polycrystalline* material by annealing. In Lee's method, the annealing of

amorphous bonding layers yields an amorphous compound bond layer (*e.g.*, abstract, paragraphs [0021], [0022], [0044], [0061], [0068]). Crystallization of amorphous bonding layers is not taught. Nor is there any suggestion of carrying out such a crystallization process to effect bonding. The bonding process of Lee is based on a chemical reaction, not a crystallization process as in the present application. In paragraph [0015], Lee states "the present invention is embodied in a method for fabricating a bonded substrate using a *selenidation* reaction to form a compound bond layer that adhesively bonds at least one active substrate to a base substrate." There is no teaching or suggestion anywhere in Lee of crystallizing an amorphous material to a polycrystalline material to form the compound bond layer. Applicants therefore submit that Lee does not anticipate independent claim 30.

Claims 101 and 102

Independent claim 102 recites, *inter alia*, depositing low temperature grown compound semiconductor bonding layers on first and second structures. Independent claim 101 further recites depositing Ga-rich low temperature grown compound semiconductor bonding layers on first and second structures. Applicants respectfully disagree with the Examiner's assertion that *compound* semiconductor bonding layers are disclosed in Lee on page 5, line 50. This line of Lee makes reference to an "elemental compound" that may be used as the first and second materials 11, 13. Applicants submit that Lee's use of the word "compound" juxtaposed with "elemental" is technically inaccurate and does not represent the disclosure of bonding layers on first and second structures comprising a "compound" semiconductor, as recited by claims 101 and 102. Upon reading the specification, one of ordinary skill in the art would recognize that Lee's "elemental compound" may be an "element" or an "elemental material," but is not a "compound" by any proper definition. As is well known in the art, a "compound" includes at least two elements bound together in definite proportions. Lee discloses "elemental selenium" and "elemental indium" as exemplary "elemental compounds" in paragraph [0060]. One of ordinary skill in the art would readily recognize that neither selenium nor indium is a compound. Only *after* the elemental bonding layers of Lee have undergone the selenidation reaction to form the bonded

structure is a compound semiconductor (e.g., In_xSe_y) formed in Lee. Applicants further point out that the addition of tellurium to a selenium layer, as disclosed in Lee, yields an alloy of the two elements and does not constitute the formation of a *compound* semiconductor bonding layer. Applicants refer the Examiner to U.S. Patent 3,723,105, "Process for Preparing Selenium-Tellurium Alloys," which describes the vapor deposition of selenium-tellurium alloy films. In summary, Lee does not disclose low temperature grown compound semiconductor bonding layers on first and second structures. Applicants therefore submit that Lee does not disclose the limitations of independent claims 101 and 102.

Since Lee does not teach each and every element of independent claims 30, 101, and 102, the reference cannot anticipate these claims or any claims depending therefrom. Applicants further submit, however, that some of the dependent claims are independently patentable over Lee.

Claims 31, 39-41, 49, 53, 80, 82, 109-110, 113, and 119

Claim 31 recites applying a pressure substantially uniformly to the combined structure during annealing. The Examiner erroneously asserted that Lee discloses this limitation in Fig. 4B. In fact, Lee teaches that the compound bond layer may be formed "without having to apply pressure to achieve the bonding." (page 3, lines 30-31) Furthermore, the pressure disclosed in Lee that occurs incidentally due to gravity on the mass of the upper substrate (page 5, lines 35-38) does not constitute the *application* of pressure to a *combined structure* that includes both first and second structures (substrates) and the bonding layers deposited thereon, as recited by the present claims.

Claim 39 and 109 recites annealing the combined structure under conditions that are sufficient to form bonds strong enough to survive subsequent processing at temperatures higher than those used during bonding. The Examiner alleges that the limitations of these claims are disclosed in the abstract of Lee. In fact, there is no discussion in the abstract about subsequent processing at higher temperatures than those used during bonding, as required by the claims.

Claims 40 and 110 recite that a bonding interface produced by the annealing is substantially optically transparent to light emitted by the combined structure. In the prior

Office Action the Examiner asserted that the abstract of Lee discloses this limitation. To the contrary, there is no teaching in the abstract, or anywhere else in Lee, that the bonding interface is optically transparent.

Claim 41 recites that a bonding interface produced by the annealing is strong enough to be substantially *unaffected* by processing of the combined structure. In the prior Office Action, the Examiner incorrectly stated that the abstract of Lee discloses this limitation. In fact, the abstract of Lee teaches that processing of the combined structure can *dissolve* the bond. A bonding interface that can be dissolved is not substantially unaffected by processing, as required by claim 41.

Claim 49 recites that the bonding layer comprises a "compound" semiconductor. Per the arguments above in reference to claims 101 and 102, this claim is independently patentable over Lee.

Claims 53 and 119 recite a bonding layer deposited by molecular beam epitaxy at a temperature of at most about 100°C. The Examiner alleged in the prior Office Action that Lee discloses this limitation on page 5, at line 50. In fact, Lee does not teach this deposition technique on page 5 or anywhere else in the specification.

Claim 80 recites that the first and second structures comprise a pseudomorphic structure, which is not disclosed anywhere in Lee.

Claim 82 recites that the bonding layer is *devoid* of polymers, ceramics, and metals. Since Lee discloses the use of metals as exemplary materials for the bonding layer (e.g., aluminum (Al), indium (In)), the reference clearly does not teach or suggest the limitations of claim 82.

Claim 113 recites annealing of the combined structure under conditions sufficient for the bonding layers to form a polycrystalline material from an amorphous layer. Per the preceding arguments in reference to claim 30, this claim is independently patentable over Lee.

In view of the amendment to claim 30 and the above remarks, Applicants respectfully request that the Examiner withdraw the rejection of claims 30-32, 36-42, 44-47, 49, 51-53, 78-80, 101-104, 108-110, 112-114, and 117-119 under 35 U.S.C. §102(b).

Rejections Under 35 U.S.C. § 103

The Examiner asserted that claims 33-35, 43, 48, 50, 101, 105-107, and 116 are unpatentable under 35 U.S.C. 103(a) over Lee in view of Malik et al. ("Malik," US 6,881, 644). Applicants respectfully disagree.

Claims 33-35, 43, 48, 50, 101, 105-107, and 116

Claims 33-35, 43, 48, and 50 depend from claim 30 and therefore include all of the limitations of claim 30. Likewise, claims 105-107 and 116 depend from claim 102 and thus contain all of the limitations of claim 102. Applicants submit that independent claims 30, 101, and 102 are patentable over Lee in view of Malik, and thus the dependent claims are also patentable. Per the preceding arguments, Lee does not disclose at least one amorphous bonding layer and the crystallization of at least a portion of the amorphous material into a polycrystalline material during annealing, as recited by claim 30. Malik also does not disclose this limitation of the claims. Claims 101 and 102 recite, *inter alia*, low temperature grown compound semiconductor bonding layers on first and second structures. Lee does not disclose this limitation, per the preceding arguments. As discussed in Applicants' response to the prior Office Action, there is no teaching anywhere in Malik of compound semiconductor bonding layers grown at low temperatures. Malik also does not disclose depositing such bonding layers on first *and* second substrates and placing the bonding layers in contact with each other, as further recited in claims 101 and 102. At best, Malik discloses a compound semiconductor layer on a first structure placed in contact with and bonded to a substrate that does not include such a bonding layer. (col. 8, lines 6 and 29-34). There is no teaching or suggestion anywhere in Malik of using low temperature grown compound semiconductor bonding layers on both first and second structures (*i.e.*, substrates).

Since the references, either alone or in combination, do not teach or suggest each and every element of independent claims 30, 101, and 102, the Examiner has not established a *prima facie* case of obviousness with respect to these claims or to claims 33-35, 43, 48, 50, 105-107, and 116, which depend therefrom. Applicants therefore

submit that claims 33-35, 43, 48, 50, 101, 105-107, and 116 are patentable over Lee in view of Malik.

Claims 33, 34, 35, 43, 48 and 50

Applicants further submit, however, that some of the dependent claims are independently patentable over Lee in view of Malik.

Claim 33 recites annealing the combined structure at a temperature of between about 300˚C and 500˚C for a time sufficient to form a (Ga,As) layer that is substantially entirely polycrystalline. There is no disclosure anywhere in Lee of using arsenic (As) as one of the materials (11, 13) for the multistacked layers (15,17), much less the formation of a (Ga,As) material from the layers. Lee also does not disclose the claimed annealing temperatures. The Examiner refers to col. 8, lines 1-10 and col. 12, lines 40-50 of Malik in the rejection. However, there is no discussion whatsoever in these sections of annealing at the claimed temperatures to form a polycrystalline (Ga,As) material. Instead, Malik describes oxidizing a porous silicon layer at temperatures of 200˚C to 700˚C to produce an oxidized film. The claimed material (Ga,As) is not even mentioned, much less the formation of a substantially entirely polycrystalline (Ga,As) material by annealing.

Claim 34 recites annealing the combined structure at a temperature of between about 500˚C and 700˚C for a time sufficient to form a (Ga,P) layer that is substantially entirely polycrystalline. There is no disclosure anywhere in Lee of using phosphorus (P) as one of the materials (11, 13) for the multistacked layers (15,17), much less the formation of a (Ga,P) material from the layers. Lee also does not disclose the claimed annealing temperatures. Once again, the Examiner refers to col. 8, lines 1-10 and col. 12, lines 40-50 of Malik in the rejection. However, there is no disclosure in these sections, or anywhere else in Malik, of annealing a combined structure at the claimed temperatures to form a polycrystalline (Ga,P) material.

Claim 35 recites annealing the combined structure at a temperature of between about 700˚C and 900˚C for a time sufficient to form a (Ga,N) layer that is substantially entirely polycrystalline. There is no disclosure anywhere in Lee of the formation of a (Ga,N) material from the layers. Lee also does not disclose the claimed annealing

temperatures. The Examiner points to col. 12, lines 1-15 of Malik in the rejection. However, there is no teaching or suggestion of forming a substantially entirely polycrystalline (Ga,N) material by annealing at a temperature of between about 700°C and 900°C in this section, or elsewhere in Malik. The claimed material is not even mentioned, much less the formation of a substantially entirely polycrystalline (Ga,N) material by annealing.

Claim 43 recites that the deposition deposits at least one of low temperature grown (Ga,As), (Ga,P), and (Ga,N) on at least one of the first and second structures. The Examiner erroneously asserts that this claim limitation is disclosed in Malik at col. 14, lines 53-67. In fact, in this section Malik teaches that it is not the bonding layer, but the *substrate* that can be made of Group III/V materials, such as gallium arsenide and gallium nitride. There is no discussion whatsoever of the deposition of low temperature grown (Ga,As), (Ga,P), and (Ga,N) *bonding layers* on the substrate.

Claim 48 recites that the annealing of the combined structure occurs at temperatures of at most about 800°C. The Examiner erroneously asserts that this limitation is disclosed in col. 12, lines 45-50 of Malik. As noted above, in this section Malik describes oxidizing a porous silicon layer at temperatures of 200°C to 700°C to produce an oxidized film. There is no teaching or suggestion by Malik to carry out the annealing of the combined structure, which includes low temperature grown semiconductor bonding layers, at temperatures of at most about 800°C.

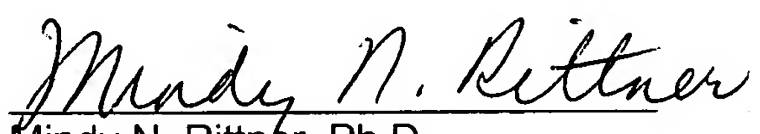
Claim 50 recites doping the bonding layer with silicon. The Examiner alleges that this limitation is disclosed in col. 8, lines 1-15 of Malik. In this section, Malik discloses silicon films. The disclosure of films composed of silicon does not constitute *doping* with silicon. As one of ordinary skill in the art would know, doping with silicon entails deliberately adding a small amount of silicon to another previously formed semiconductor in order to modify the electronic properties of the semiconductor. Doping of the claimed bonding layers with silicon is neither taught nor suggested by Malik.

In view of the preceding arguments, Applicants respectfully request that the Examiner withdraw the rejections to claims 33-35, 43, 48, 50, 101, 105-107, and 116 under 35 U.S.C. § 103(a).

Conclusion

Applicants respectfully submit that all of the pending claims are in condition for allowance. If for any reason the Examiner is unable to allow the application in the next Office action and believes that a telephone interview would be helpful to resolve any remaining issues, the Examiner is invited to contact the undersigned.

Respectfully submitted,



Mindy N. Rittner, Ph.D.
Registration No. 57,803
Agent for Applicants

BRINKS HOFER GILSON & LIONE
P.O. BOX 10395
CHICAGO, ILLINOIS 60610
(312) 321-4200